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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/815,792 | 04/02/2004 | Jae-Bon Koo | 6161.0121.US | 9923 |

58027 7590 03/20/2006

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| EXAMINER | |
|---|---|
| WON, BUMSUK | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2879 | |

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/815,792 | KOO ET AL. | |
| | Examiner | Art Unit | |
| | Bumsuk Won | 2879 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *2 and 11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04, 08/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 1 and 3-10 in the reply filed on 2/24/2006 is acknowledged.

### *Claim Rejections - 35 USC § 112*

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "the drain offset regions" in line 1. There is insufficient antecedent basis for this limitation in the claim. For examining purpose, the drain offset region will be assumed as a part of the drain region.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5-8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (JP 2001-109399) which is the Applicant's admitted prior art.

Regarding claim 1, Yamada discloses a flat panel display (figures 1-3), comprising: R, G and B unit pixels (110B, R, G), each pixels including a transistor with source/drain regions (figure 2, 30, 40), wherein transistors of at least two unit pixels of R, G, B unit pixels have drain regions (43c, 43d) of different geometric structures (paragraphs 37-41).

Regarding claim 3, Yamada discloses the drain regions (43c, 43d) of the transistors of the R, G and B unit pixels are of a construction having a same length and a different width from one another (paragraph 40-41).

Regarding claim 5, Yamada discloses each unit pixel includes an organic EL device (60) driven by the transistor (paragraph 33), and a drain region (43c, 43d) of a transistor to drive the organic EL device having the highest luminous efficiency of the organic EL device among the transistors in the unit pixels has a narrower width compared to widths of drain regions of transistors to drive organic EL device having a relatively lower luminous efficiency (paragraphs 37-41).

Regarding claim 6, Yamada discloses the drain regions (43c, 43d) of the transistors include offset regions (43c) having different geometric structures from one another, respectively (paragraphs 37-41).

Regarding claim 7, Yamada discloses each unit pixel includes an organic EL device (60) driven by the transistor (paragraph 33), and a drain offset region (43c) of a transistor to drive the organic EL device having the highest luminous efficiency of the organic EL device among the transistors in the unit pixels has a narrower width compared to widths of drain offset regions of transistors to drive organic EL device having a relatively lower luminous efficiency (paragraphs 37-41).

Regarding claim 8, Yamada discloses the drain offset regions (43c) of the transistors of the R, G and B unit pixels are of a construction having a same length and a different width from one another (paragraphs 40-41).

Regarding claim 10, Yamada discloses each unit pixel includes an organic EL device (60) driven by the transistor (paragraph 33), and channel layers (43c) of the transistors controlling currents supplied to the organic EL device of the unit pixels are of same size (paragraphs 37-41, each R, G and B will have its own size which are same size within each R, G and B).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (JP 2001-109399) which is the Applicant's admitted prior art in view of Park (US 7,002,302).

Regarding claim 4, Yamada discloses all of the claimed limitations except for the drain regions of the transistors are zigzag shapes.

Park discloses a flat panel display (column 1, lines 15-19) having drain regions (figure 8, 825 and 827) of transistors (figure 8) being zigzag shapes (column 8, lines 29-31), for the purpose of increasing resistance of drain regions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the drain regions of transistors being zigzag shapes disclosed by Park in the flat panel display disclosed by Yamada, for the purpose of increasing resistance of drain regions.

Regarding claim 9, Yamada discloses all of the claimed limitations except for the drain offset regions of the transistors are zigzag shapes.

Park discloses a flat panel display (column 1, lines 15-19) having drain offset regions (figure 8, 827) of transistors (figure 8) being zigzag shapes (column 8, lines 29-31), for the purpose of increasing resistance of drain offset regions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the drain regions of transistors being zigzag shapes disclosed by Park in the flat panel display disclosed by Yamada, for the purpose of increasing resistance of drain offset regions.

***Contact information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bumsuk Won whose telephone number is 571-272-2713. The examiner can normally be reached on Monday through Friday, 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bumsuk Won
Patent Examiner

JOSEPH WILLIAMS
PRIMARY EXAMINER